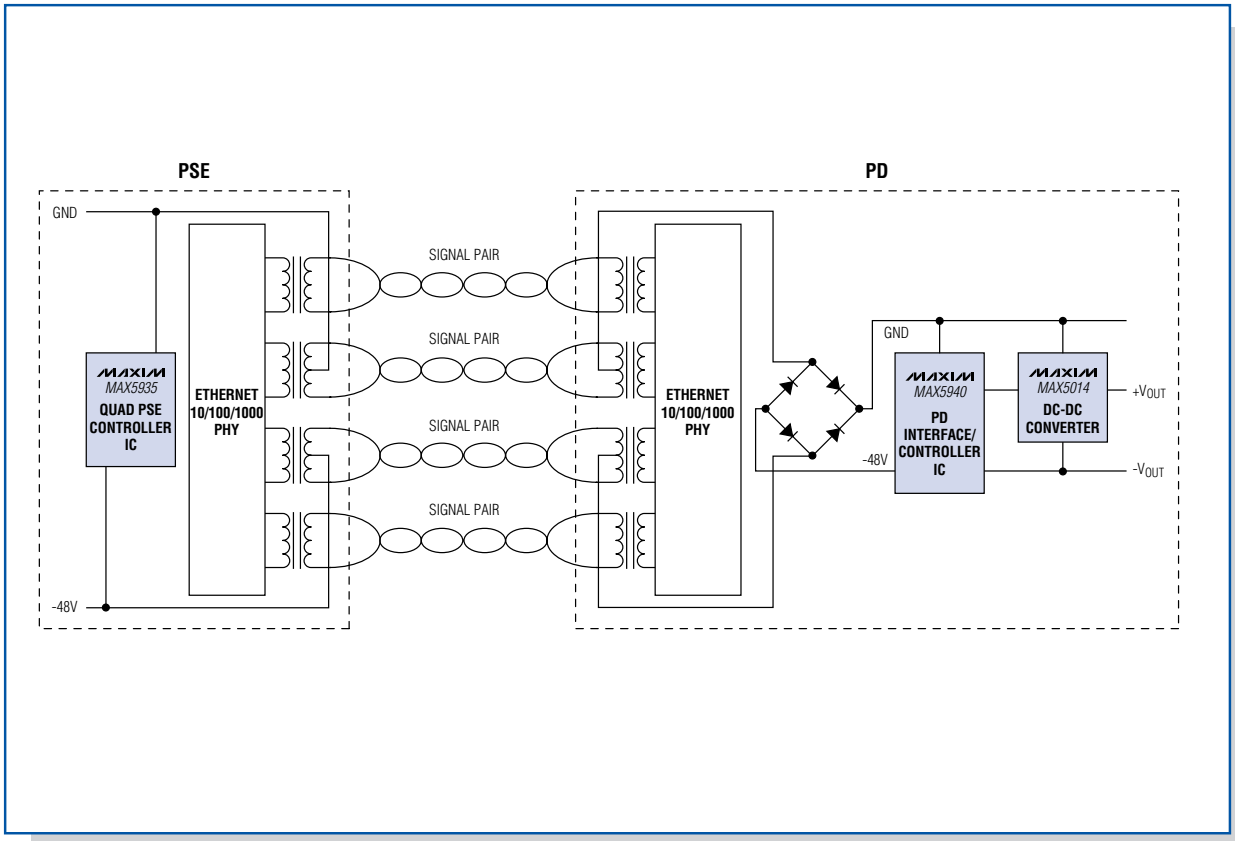
DALLAS SEMICONDUCTOR MAXIM

Engineering Journal

Volume Fifty-Three



A PD operating with Gigabit Ethernet must be backward compatible with midspan PSE applications, and therefore receive power from an endpoint PSE switch. (See article inside, page 9.)

News Briefs

MAXIM REPORTS REVENUES AND EARNINGS GROWTH FOR THE FOURTH QUARTER AND 2004 FISCAL YEAR

Maxim Integrated Products, Inc., (MXIM) reported net revenues of $421.0 million for its fiscal fourth quarter ending June 26, 2004, a 42.7% increase over the $295.0 million reported for the fourth quarter of fiscal 2003 and a 13.8% increase over the $370.0 million reported for the third quarter of fiscal 2004. Net income for the quarter was $124.7 million, a 52.5% increase over the $81.7 million reported last year and a 14.2% increase over the $109.2 million reported for the third quarter. Diluted earnings per share were $0.36 for the fourth quarter, a 50.0% increase over the $0.24 reported for the same period a year ago and a 16.1% increase over the $0.31 reported for the third quarter of fiscal 2004.

For the 2004 fiscal year, Maxim reported net revenues of $1.439 billion compared to $1.153 billion for last year, a 24.8% increase. Net income for the 2004 fiscal year was $419.8 million compared to $309.6 million reported for fiscal 2003. Diluted earnings per share grew 31.9% from $0.91 per share reported for fiscal 2003 to $1.20 per share in fiscal 2004.

During the quarter, cash and short-term investments increased $7.6 million after the Company repurchased 2.1 million shares of its common stock for $100.1 million, paid dividends of $25.8 million, and acquired $68.9 million in capital equipment. During fiscal year 2004, the Company repurchased 12.4 million shares of its common stock for $601.2 million, paid dividends of $104.6 million, and acquired $231.6 million in capital equipment.

Accounts receivable increased $34.7 million in the fourth quarter to $197.2 million due to the increase in net revenues, and inventories increased $14.4 million to $117.8 million.

Research and development expense was $87.8 million or 20.8% of net revenues in the fourth quarter, compared to $77.3 million or 20.9% of net revenues in the third quarter of fiscal 2004. The increase in research and development expense in the fourth quarter was due to a one-time employee bonus, hiring additional engineers, and increased expenses to support the Company's new product development efforts. Selling, general and administrative expenses increased from $23.5 million in the third quarter to $26.4 million in the fourth quarter but decreased as a percentage of net revenues from 6.4% to 6.3%.

In the fourth quarter, the Company recorded a $17.5 million one-time bonus to employees below the managing director level, which increased cost of goods sold by $5.9 million, increased research and development expense by $9.5 million, and increased selling, general and administrative expenses by $2.1 million.

Fourth quarter bookings were approximately $535 million, a 9% increase over the third quarter's level of $488 million. Turns orders received in the quarter were approximately $170 million, a 10% decrease from the $189 million received in the prior quarter (turns orders are customer orders that are for delivery within the same quarter and may result in revenue within the same quarter if the Company has available inventory that matches those orders). Bookings increased in all geographic regions except Europe, with the strongest bookings growth coming from the Pacific Rim and Japan.

Jack Gifford, Chairman, President, and Chief Executive Officer, commented on the fiscal year: "Fiscal 2004 was a strong growth year for Maxim. Orders improved each quarter, both sequentially and year-over-year. Orders for our power management products collectively grew 68% year-over-year, and orders for our communications, data converter, and mixed-signal product lines grew year-over-year 63%, 72%, and 45%, respectively."

Mr. Gifford continued: "Our manufacturing capacity expansions in both our wafer fab and end-of-line operations are proceeding according to plan. Our San Antonio wafer fab began production in the fourth quarter, and our new end-of-line facility in Thailand went on line at the beginning of Q105. We are well equipped to respond to the continued growth in demand for our products that we forecast for fiscal 2005."

Mr. Gifford added: "We forged important strategic alliances with major electronics manufacturers this year and secured significant design wins in a myriad of market areas, including multifunction cellular phones, portable audio players, PDAs, servers, displays, and storage devices. These design wins will help fuel our future growth."

Mr. Gifford concluded: "The Company's Board of Directors has declared a quarterly cash dividend of $0.08 per share. Payment will be made on August 31, 2004 to stockholders of record on August 16, 2004."

For the complete Q404 press release, including safe harbor information, go to: www.maxim-ic.com/AboutMaxim/Investor.htm

Dynamic performance requirements for high-performance ADCs and RF components in digital receiver applications

Most digital receivers place demanding requirements on high-performance analog-to-digital converters (ADCs) and analog components. In cellular base-station digital receivers, for example, sufficient dynamic range is needed to handle high-level interferers (or blockers), while properly demodulating the lower level desired signal. The MAX1418 (15-bit, 65Msps) or MAX1211 (12-bit, 65Msps) ADC, in combination with the MAX9993 (2GHz) or MAX9982 (900MHz) integrated mixer, provides exceptional dynamic range for two of the most critical stages in a receiver line-up. In addition, the MAX2027 and MAX2055 IF digital variable-gain amplifiers (DVGAs) provide exceptionally high third-order output intercept performance (OIP3) with the gain-adjustment range required for many applications.

A cellular base station (base transceiver station, or BTS) consists of many different hardware modules including a transceiver (TRx), which performs the RF receiver (Rx) and transmitter (Tx) functions. In the older analog AMPS and TACS BTSs, one TRx handles a duplexed Rx and Tx RF carrier. Many transceivers are needed to provide enough carriers to obtain the required calling coverage. Analog technology is being replaced by CDMA and W-CDMA worldwide, and gradually by GSM also, which was adopted by Europe over a decade ago. In CDMA, many callers utilize the same RF frequency, which allows a single transceiver to handle many callers' signals simultaneously. Various CDMA and GSM designs exist today, and methods to reduce their cost and power are continuously being sought by BTS manufacturers. Optimizing single-carrier solutions or developing multicarrier receivers can accomplish this. **Figure 1** illustrates the main blocks in a subsampling receiver architecture commonly used in BTS equipment.

The MAX9993 (2GHz) and MAX9982 (900MHz) mixers provide gain and high linearity coupled with low noise figure, allowing the designer to eliminate lossy, passive mixers in many designs. The MAX2027 and MAX2055 are designed to operate in the first or second IF stages of the receiver. The MAX2027 offers +35dBm OIP3 and the MAX2025 offers +40dBm OIP3 over the entire gain-adjustment range. Even though the MAX1418 (15-bit, 65Msps) and MAX1211 (12-bit, 65Msps) data converters are illustrated in Figure 1, other speed grades satisfying most applications are included in both converter families. If the second downconversion is eliminated (shown in dashed lines), the figure depicts a single downconversion architecture.

Low-noise ADC (MAX1418)

For the subsampling receiver architecture shown in Figure 1, stringent noise and distortion requirements are placed on the ADC. In receiver applications, the lower level desired signal is digitized alone or in the presence of an unwanted signal(s) that can be significantly larger in amplitude. To properly design the receiver, the ADC's

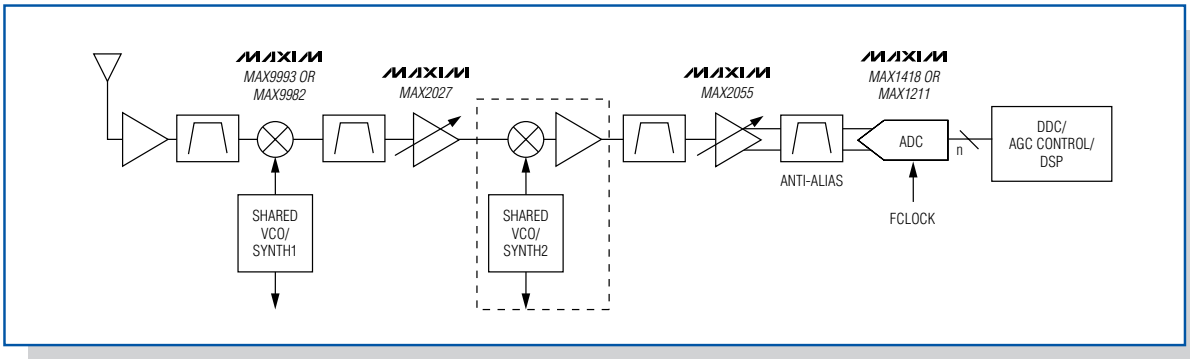


Figure 1. One of two diversity branches is shown for a representative double down-conversion architecture.

Table 1. MAX1418 electrical characteristics

Parameter	Condition	Symbol	Typ Value	Units
Resolution	—	N	15	Bits
Analog input range	—	V_{ID}	2.56	V_{P-P}
Differential input resistance	—	R_{IN}	1	kΩ
AC specifications	f_{CLK} = 65Msps	—	—	—
Thermal + quantization noise floor	Analog input < -35dBFS	Nfloor	-78.2	dBFS
Signal-to-noise-ratio analog input = -2dBFS	f_{IN} = 70MHz	SNR	73.6	dB
Spurious-free dynamic range analog input = -2dBFS	f_{IN} = 70MHz	SFDR	88	dB
Signal-to-noise-and-distortion analog input = -2dBFS	f_{IN} = 70MHz	SINAD	73.3	dB

effective noise figure must be determined under these two signal extremes. The converter's noise figure is determined by comparing its total noise power to the thermal noise floor. For small analog input signals, the thermal plus quantization noise power dominate the ADC's noise floor, which is used to approximate the ADC's effective noise figure (NF).

In practice, once the ADC's effective noise figure is known in the small signal condition and the cascaded noise figure of the analog circuitry (RF and IF) is determined, the minimum power gain ahead of the ADC is selected to meet the required receiver noise figure. The amount of power gain places an upper limit on the maximum blocker, or highest interference level that the receiver can tolerate before the ADC overloads. For BTS applications, the ADC often does not have sufficient dynamic range to meet both the noise figure requirements (receiver sensitivity) and maximum blocker requirements without implementing automatic gain control (AGC). The AGC can be included either in the RF stages, IF stages, or both.

Other converters in the MAX1418 family are optimized for baseband performance where $f_{INPUT} < f_{CLOCK}/2$. Operating in this frequency range and using these baseband-optimized parts provide the best possible converter dynamic range. These converters include the MAX1419 (optimized for a 65Msps clock rate) and the MAX1427 (optimized for an 80Msps clock rate), both with SFDR performance equal to 94.5dBc at baseband.

The following example uses the MAX1418 specifications listed in **Table 1**.

The MAX1418 can be used with a 14-bit interface by not connecting the LSB. If so used, there is a slight SNR performance penalty and the SFDR performance remains essentially unaffected.

Figure 2 illustrates the ADC noise contribution in the absence of a large-level blocker. Assume all analog circuitry in front of the ADC has a cascaded noise figure of 3.5dB. As a first approximation, suppose a designer's goal is for the ADC to degrade the overall receiver noise figure by no more than 0.2dB to meet some target sensitivity in a CDMA base-station receiver. This noise figure value should provide sufficient margin to the air-interface requirements, which is also dependent on the final detector's EB/NO (bit energy to noise power spectral-density ratio) requirement. If the MAX1418 thermal-plus-quantization noise-floor value from Table 1 is used, an equivalent noise figure of 26.9dB can be calculated when the device is clocked at 61.44Msps (50x chip rate). The ADC noise in the 1.23MHz CDMA channel bandwidth is 14dB lower than the noise in the Nyquist bandwidth due to the processing gain achieved. An overall gain of 36dB is needed to achieve the desired cascaded receiver noise figure value of 3.7dB.

With 36dB gain ahead of the ADC, a maximum single-tone blocker level above -30dBm at the antenna terminal exceeds the ADC full-scale input. The cdma2000® cellular base-station standard specifies a maximum allowable blocker level of -30dBm at the antenna terminal. For this example, 6dB of gain reduction is used to increase the largest allowable blocker signal applied to the ADC, providing margin to the standard's specification. Assuming 2dB of headroom is allowed, 6dB of gain reduction results in a maximum blocker level of -26dBm at the antenna and +4dBm at the ADC input (see **Figure 3**). The cellular standards allow 3dB of degradation overall (noise plus

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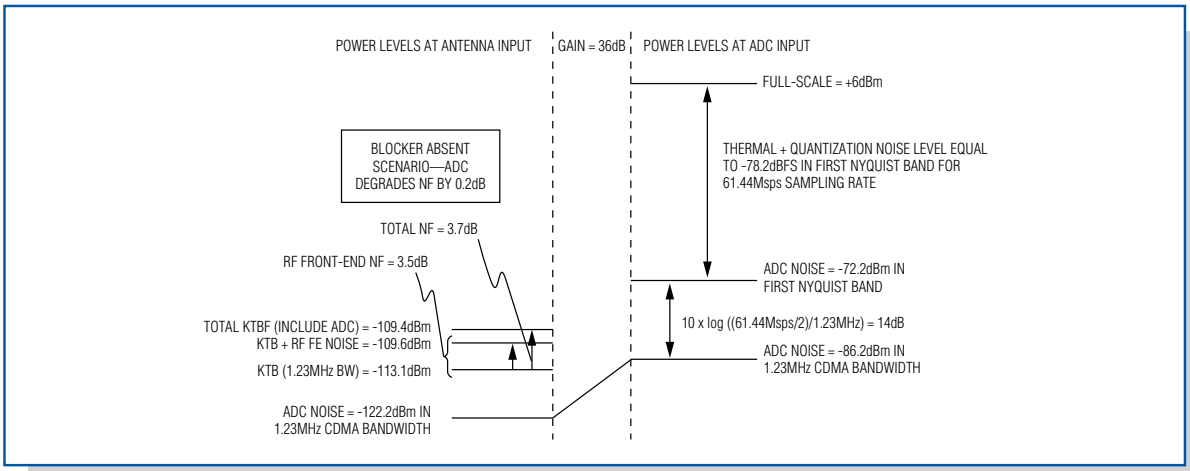

Figure 2. ADC noise contribution is shown for no blocker present.

distortion) relative to reference sensitivity when a single-tone blocker is present. The allocation of individual noise and distortion components is left to the designer.

Suppose the designer allows the RF front-end cascaded noise plus distortion to degrade the NF by 1dB (from the nominal 3.5dB) when the blocker is present with 6dB of AGC applied. With only 30dB of gain in front of the ADC, and an effective noise figure of 29.4dB determined by the ADC SNR performance, the cascaded receiver noise figure is 5.7dB in the 'blocked condition.' This is a 2dB degradation from the 3.7dB noise figure calculated for receiver sensitivity. Because this calculation does not take into account the spurious performance, an additional 1dB of degradation can be allowed for the ADC's spurious-free dynamic range (SFDR) performance. Instead of calculating noise and SFDR contributions separately, SINAD could have been used to compute the effective NF when a blocker signal is present.

MAX1211 allows single downconversion architecture

The subsampling architecture can be used with a single downconversion architecture if sufficient SNR and SFDR performance can be obtained from the converter at higher IF frequencies. The MAX1211 is a 12-bit, 65Msps converter designed with this architecture in mind, along with pin-compatible 80Msps and 95Msps versions that will soon be released. This family of converters allows direct-IF sampling for input frequencies up to 400MHz. Their advanced features include: differential or single-ended clock input; 20% to 80% clock duty cycle; data valid indicator allowing the simplification of clock and

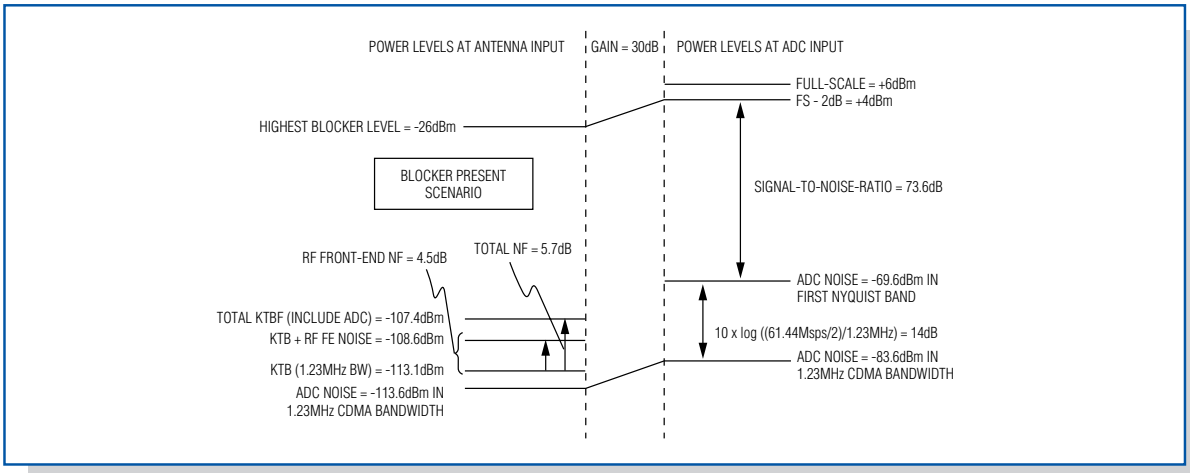

Figure 3. ADC noise contributions detailed for various blockers present.

Table 2. MAX1211 electrical characteristics

Parameter	Condition	Symbol	Typ Value	Units
Resolution	—	N	12	Bits
Analog input range	—	V_{ID}	2	V_{P-P}
Differential input resistance	—	R_{IN}	15	kΩ
AC specifications	f_{CLK} = 65Msps	—	—	—
Thermal + quantization noise floor	Analog input < -35dBFS	Nfloor	69.3	dBFS
Signal-to-noise-ratio analog input = -0.5dBFS	f_{IN} = 70MHz f_{IN} = 175MHz	SNR	68.3 66.8	dB
Spurious-free dynamic-range analog input = -0.5dBFS	f_{IN} = 70MHz f_{IN} = 175MHz	SFDR	82.4 79.8	dB
Signal-to-noise-and-distortion analog input = -0.5dBFS	f_{IN} = 70MHz f_{IN} = 175MHz	SINAD	68.1 66.5	dB

data timing; and two's complement or gray code digital-output data format all in a small, 40-pin TQFN package (6mm x 6mm x 0.8mm). See **Table 2** for the typical MAX1211 AC specifications illustrating the superb AC performance for an analog input frequency of 175MHz.

There are significant advantages gained when choosing single downconversion instead of double downconversion. By eliminating the second downconversion mixer, second-IF gain stages, and second LO synthesizer circuitry, the parts count and board space can be reduced by approximately 10% and cost by $10 to $20.

Spurious considerations for different architectures

If saving parts count, board space, power, and cost do not provide enough incentive, the following example illustrates the frequency-planning advantage gained when using the MAX1211 in a single downconversion architecture. Suppose a cdma2000 receiver is designed to operate in the PCS frequency band. For a sample rate of 61.44Msps and synthesizer reference frequency of 30.72MHz, choose a first IF frequency centered in the sixth Nyquist band at 169MHz having a bandwidth of approximately 1.24MHz. Using the same first IF center frequency of 169MHz, the double downconversion (DDC) architecture assumes that a second IF frequency is centered in the second Nyquist band at 46.08MHz.

Table 3 lists the spur search assumptions for an RF carrier near the upper end of the PCS band for the single-carrier, single downconversion (SDC), and DDC architectures. For the SDC architecture, the spur search resulted in 134 total spurs in the RF receive band, receive image band, IF band, and IF image band. Most of these spurs are high order, and do not degrade the receiver's performance. For the DDC architecture, this spur search results in over 2400 spurs, which is 18 times more than what was calculated for the SDC architecture. These spurious products occur in the RF receive band, receive image band, first IF band, first IF image band, second IF band, and second IF image band. The spurs resulting from combinations of higher clock harmonics and synthesizer reference frequencies are relatively easy to reduce through good board layout practices and filtering. However, a significant number of lower order spurs are difficult to minimize.

IF amplifiers (MAX2027 and MAX2055)

Maxim also offers high-performance IF amplifiers with digital variable-gain control in 1dB increments. The MAX2027 is a digital variable-gain amplifier (DVGA) with single-ended input/single-ended output for frequencies ranging from 50MHz to 400MHz. This DVGA offers a low noise figure of 5dB at maximum gain. The MAX2055 is a single-ended input/differential output DVGA meant to drive high-performance ADCs for frequencies ranging from 30MHz to 300MHz. A step-up transformer can be used between the differential output of the MAX2055 and the ADC differential input. The transformer is driven differentially, thus optimizing the transformer performance and balance between the output signals. Both DVGAs operate from 5V bias; the MAX2027 offers +35dBm OIP3 and the MAX2025 offers +40dBm OIP3 over the entire gain-adjustment range. Refer to the associated data sheets on Maxim's website for additional detail at www.maxim-ic.com/max2027 and www.maxim-ic.com/max2025.

Table 3. Spur search assumptions for SDC and DDC architectures.

SDC	DDC	Parameter	Value
X	X	Receive band	1904.3800MHz to 1905.6200MHz
X	X	Clock frequency	61.4400MHz
X	X	Max clock harmonic	30
X	X	Synthesizer reference frequency	30.7200MHz
X	X	Max synthesizer harmonic	40
X	X	First injection LS	1736.000MHz
X	X	Max first LO harmonic	5
X	X	Receive image band	1566.3800MHz to 1567.6200MHz
X	X	First IF band	168.3800MHz to 169.6200MHz
	X	Second injection LS	122.9200MHz
	X	Max second LO harmonic	5
	X	First IF image band	76.2200MHz to 77.4600MHz
	X	Second IF band	45.4600MHz to 46.7000MHz

High-linearity mixers (MAX9992 and MAX9983)

In receiver circuits, mixers are subjected to large input signals that place stringent requirements on their performance. Ideally, the mixer's output-signal amplitude and phase are proportional to the input signal's amplitude and phase, and are independent of the LO signal characteristics. Using this assumption, the amplitude response of the mixer is linear for the RF input and is independent of the LO input.

However, mixer nonlinearities produce undesired products called spurious responses, caused by undesired signals reaching the mixer's RF input port and producing a response at the IF frequency. When they interfere with the desired IF frequency, the mixing mechanism can be described by:

$$f_{IF} = \pm mf_{RF} \pm nf_{LO}$$

where IF, RF, and LO refer to the signals at designated ports, respectively; m and n are integer harmonics of both the RF and LO frequencies that mix to create numerous combinations of spurious products.

Integrated (or active) balanced mixer designs, such as MAX9992 and MAX9983, are becoming more popular as their performance rivals that of passive mixer solutions. Balanced mixers reject certain spurious responses when m or n is even, resulting in excellent second-order harmonic performance. Ideal double-balanced mixers reject all responses where m or n (or both) is even. The IF, RF, and LO ports are mutually isolated in all double-balanced mixers. With properly designed baluns, these mixers can have overlapping RF, IF, and LO bands. The MAX9992 and MAX9983 both feature gain, low noise figure, integrated LO buffer, low LO drive, LO switch allowing two LO frequency inputs, superb LO noise performance, and integrated RF baluns on the RF and LO ports.

Maxim's mixers have built-in LO buffers with superb LO noise performance that ease the input LO power requirements driving them. LO noise reciprocally mixes with high-level input blocking signals that desensitize the receiver. Both the MAX9992 and MAX9983 have low noise LO buffers designed to have minimal impact on receiver desensitization when blockers are present. For example, suppose the VCO providing the injection signal has a sideband noise performance of -145dBc/Hz. The typical LO noise performance for the MAX9993 is -164dBc/Hz, so the composite sideband noise performance is degraded by only 0.05dBc/Hz to -144.95dBc/Hz. This way, the user benefits from needing only to provide a low-level LO injection signal to the mixer. The user can also be assured that the reciprocal mixing performance of the receiver is not degraded due to the MAX9993's LO buffer performance.

A particularly troublesome second-order spurious response, called the half-IF (1/2 IF) spurious response, is defined for the mixer indices of (m = 2, n = -2) for low-side injection, and (m = -2, n = 2) for high-side injection. For low-side injection, the input frequency that creates the half-IF spurious response is located below the desired RF frequency by an amount $f_{IF}/2$ from the desired RF input frequency (see **Figure 4**). The desired RF frequency is represented by 1909MHz and, in combination with the

LO frequency of 1740MHz, the resulting IF frequency is 169MHz. Though the CDMA RF and IF carrier occupies a 1.24MHz bandwidth, it is illustrated as a single frequency indicating the center carrier frequency. For this example, the undesired signal at 1824.5MHz causes a half-IF spurious product at 169MHz.

Verify:

$2 \times f_{HALF\text{-}IF} - 2 \times f_{LO} =$

$2 \times (f_{RF} - f_{IF}/2) - 2 \times (f_{RF} - f_{IF}) =$

$2 \times f_{RF} - 2 \times f_{IF}/2 - 2 \times f_{RF} + 2 \times f_{IF} = f_{IF}$

Results in:

2 x 1824.5MHz - 2 x 1740MHz = 169MHz

The amount of rejection, called the 2 x 2 spurious response, can be predicted from the mixer's second-order intercept point, IP2. The 2 x 2 IMR or spurious values in **Figure 5** are taken from the MAX9993 data sheet. Note the signal levels in the figure are referred to the input of the mixer for which the input IP2 (IIP2) performance is calculated. Such superb level of 2 x 2 performance results in the following:

$IIP2 = 2 \times IMR + P_{SPUR} = IMR + P_{RF}$

$= 2 \times 70dBc + (-75dBm) = 70dBc + (-5dBm)$

$= +65dBm$

Similarly, the MAX9982 900MHz active mixer provides typical $2_{RF} - 2_{LO}$ spurious response equal to 65dBc under similar conditions, which results in:

$IP2 = 2 \times IMR + P_{SPUR} = IMR + P_{RF}$

$= 2 \times 65dBc + (-70dBm) = 65dBc + (-5dBm)$

$= +60dBm$

Image-reject filters used in the RF path immediately ahead of the mixer attenuate any amplifier harmonics. The noise filter in the LO path attenuates harmonics caused by the LO injection source. High-level input signals create distortion or intermodulation products and can be quantified by calculating the intercept point, either at the input or output of the device or system. For the case in which the mixer LO power is held constant, the order of the intercept point or distortion product is determined only by the RF multiplier. It is not determined by the LO multiplier, because variations in the RF signal are the only ones of concern. The order refers to how fast the amplitudes of the distortion products increase with a rise in input level.

Conclusion

It has been shown that the MAX1418 15-bit ADC offers excellent noise performance, resulting in low required receiver gain. Thus, it withstands higher blocker or interference levels with minimum AGC. The MAX1211 ADC family is ideally suited for a single-conversion receiver architecture with first IF input frequencies up to 400MHz. In addition, the MAX9992 and MAX9983 RF mixers provide the desired linearity, along with low noise figure and sufficient power gain, to eliminate the need for passive mixers in many of today's receiver designs. The MAX2027 provides approximately +35dBm OIP3 and the MAX2025 provides approximately +40dBm over the entire gain-adjustment range. A receiver lineup incorporating these components can achieve a high level of performance in a very cost-effective solution.

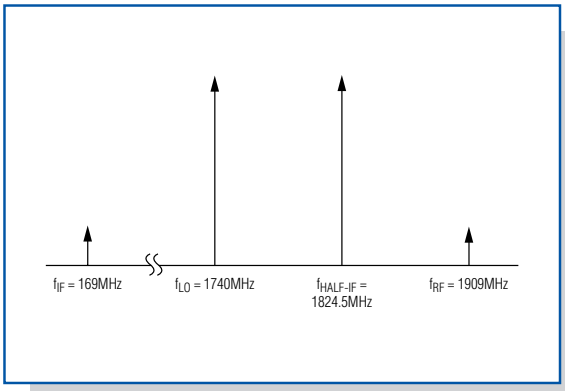

Figure 4. Frequency locations are shown for desired (f_{RF}, f_{LO}, f_{IF}) and undesired ($f_{HALF\text{-}IF}$) frequencies.

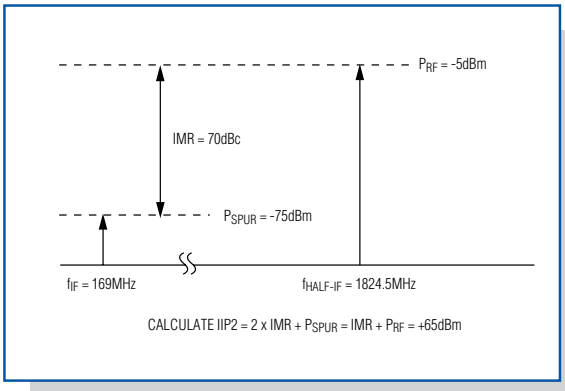

Figure 5. Second-order intercept values are calculated for signals referred to mixer input, IIP2.

New Ethernet systems distribute DC power with data

The universal network is coming to an RJ-45 jack near you, carrying power with your packets!

Power-over-Ethernet (PoE) is a power-distribution technique recently approved as IEEE standard 802.3af. It allows that ubiquitous and universal network called the Ethernet to carry DC power along with your data packets. The recent ratification of this IEEE standard appears to be the first instance in which a universal power jack or plug has been defined for worldwide use. It means that local AC power is no longer needed for all network-attached devices that need continuous power—such as IP phones, wireless access nodes, and web-surveillance cameras. It also means that the devices do not have to be placed near wall outlets, and means that power cables can be eliminated.

In PoE systems, a client device that receives power over an existing Ethernet network is called a powered device (PD). The device that delivers power to the PD is called power-sourcing equipment (PSE). Power consumption for the PD is limited to 12.95W, and PSE outputs are limited to 15.4W per RJ-45 port. Each PD can expect to draw a maximum continuous current of 350mA, assuming the Ethernet link cable and physical layer device (PHY) transformers are well balanced.

To accommodate the voltage drop that takes place along a CAT-5 Ethernet link (up to 100m long), the IEEE standard specifies different power ratings for PD and PSE. The longer links exhibit a significant drop, which obliges the PSE to output more than the nominal 48VDC to maximize power available to the PD. Therefore, voltages as high as 57VDC can be seen anywhere along an Ethernet link.

Most PoE networks can be implemented with an endpoint or midspan PSE. An endpoint PSE integrates an Ethernet switch and power source in a single device, and is situated at the other end of the Ethernet link. This PSE type is the most convenient way to implement a PoE network, as power is already inline at the endpoint of an Ethernet link. Such Ethernet switches are sometimes referred to as having "inline power" (see **Figure 1**). Endpoint PSEs are ideal for new infrastructure deployments.

For existing Ethernet networks that cannot justify such a complete overhaul, power can be injected into the Ethernet link using the midspan PSE method. Midspan PSE provides power over the “spare pairs” in the CAT-5 cable—an approach that can be cost effective if only a few Ethernet devices need power. Such a case is the 4 to 24 ports in a local area that are part of a system comprising a larger multiport network (**Figure 2**).

Endpoint PSE differs from midspan PSE in its option to deliver power either combined with the signal over the same pair of wires, or over the spare pairs. In general, a PSE must be able to provide power over the signal pairs or the spare pairs, but not both.

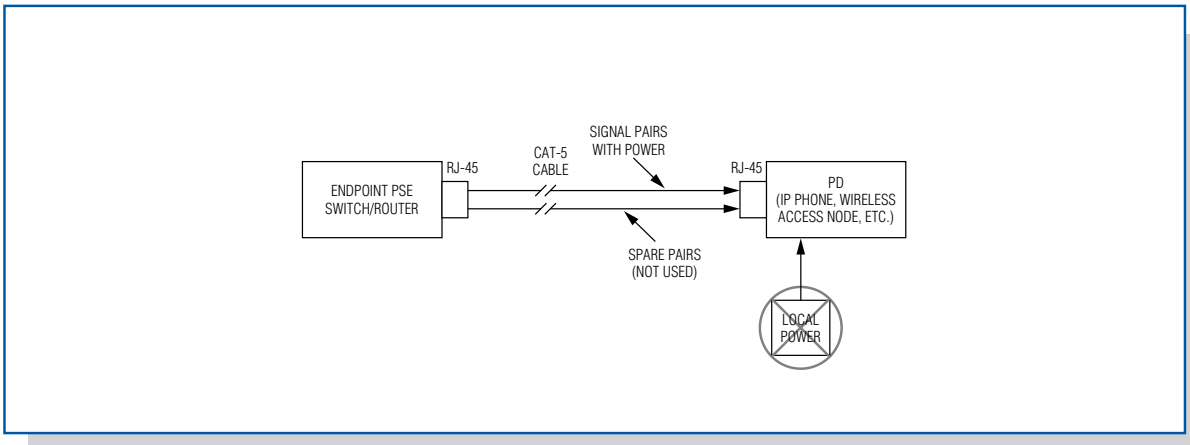

Figure 1. For endpoint PSE and PD devices, power is delivered over the signal pairs.

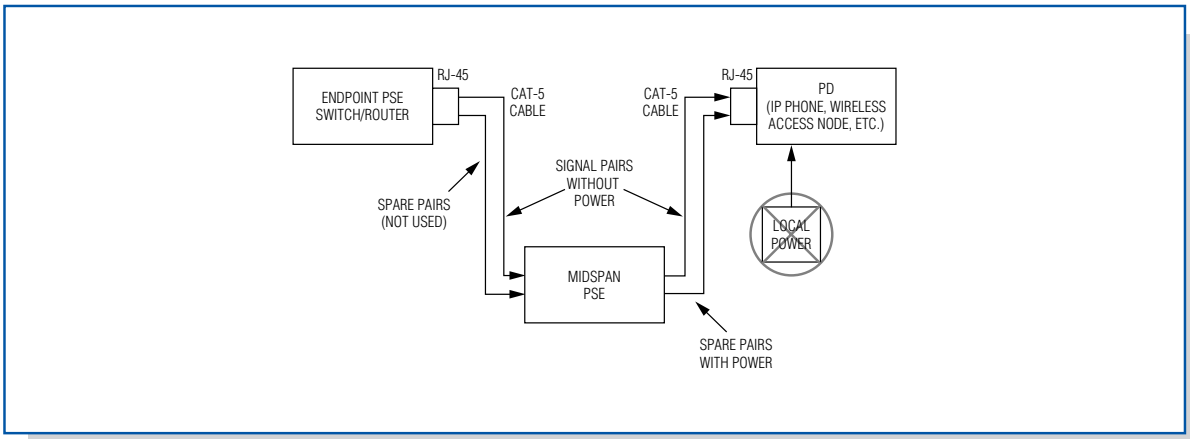

Figure 2. For midspan PSE and PD devices, power is delivered over the spare pairs.

Simple as they seem, such systems entail considerable design effort. They must include safeguards to ensure backward compatibility with devices that do not expect to see 48VDC on their Ethernet connection. The IEEE 802.3af standard covers backwards compatibility and, by including optional features for powering Ethernet networks, it also looks forward. This article covers what a designer should know in developing products destined to operate in new or existing systems—i.e., products expected to migrate towards Gigabit Ethernet or 1000BASE-T/TX.

What about Gigabit Ethernet?

Gigabit Ethernet works with endpoint PSEs, but not midspan PSEs, because it uses all four pairs within the CAT-5 cable for data transport. In contrast, 10BASE-T and 100BASE-TX use only two pairs for data (wires 1-2 and 3-6), leaving the spare pairs (wires 4-5 and 7-8) available for midspan power injection. To provide inline power for Gigabit Ethernet, therefore, endpoint PSE switches are required.

CAT-3 cable is supported by the IEEE 802.3af standard because it was originally used with 10BASE-T systems. To maximize signal integrity in new deployments, however, we recommend use of the highest rating of Ethernet cabling available (CAT-5e or CAT-6). This is because cabling infrastructures typically represent a ten-year investment. Gigabit Ethernet (1000BASE-T, specifically) requires CAT-5 cabling, but some applications using CAT-5 and Gigabit Ethernet switches have proven marginal. Consequently, the latest 1000BASE-TX standard requires CAT-6, while the original 1000BASE-T standard requires CAT-5.

Detection of PDs

When connected to its Ethernet links, the PSE must detect whether each of the Ethernet devices requires power. The PDs must therefore exhibit characteristics beyond those of a legacy Ethernet device. To accomplish this detection, the PSE makes V-I measurements while probing the signal wires with a current-limited voltage of 2.7V to 10.1V. **Table 1** lists the criteria a PD must have for

Table 1. For a valid-PD signature, all criteria below must be detected by a midspan or endpoint PSE.

Parameter	Conditions (V)	Minimum	Maximum
V-I slope (at any chord of 1V or greater)	2.7 to 10.1	23.75kΩ	26.25kΩ
Voltage offset	—	—	1.9V
Current offset	—	—	10µA
Input capacitance	2.7 to 10.1	0.05µF	0.12µF
Input inductance	2.7 to 10.1	—	100µH

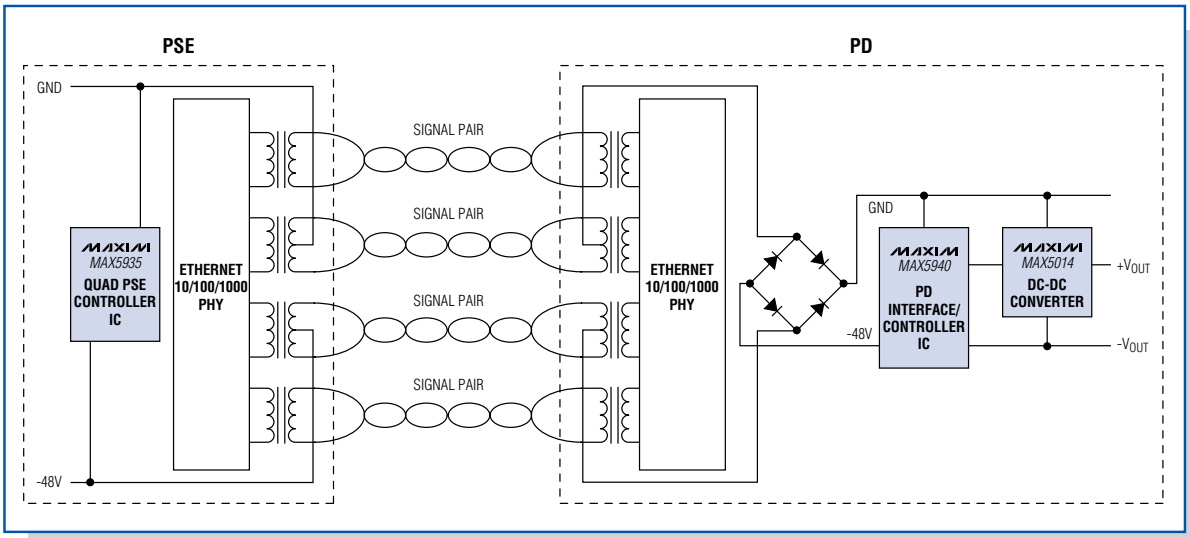

Figure 3. A PD operating with Gigabit Ethernet must be backward compatible with midspan PSE applications, and therefore receive power from an endpoint PSE switch.

detection as a valid PD. The 1.9V series offset allowed is a consequence of the diode bridges typically used to control voltage polarity. Two such bridges per PD are required, as the PD must be backward compatible with midspan PSE applications (**Figure 3**). The 10µA current offset is typically due to leakage within the PD. **Table 2** lists another set of criteria, for which any detection fails an Ethernet device by making it an invalid PD.

Power classification of PDs

The driver that first started the movement to combine power with Ethernet networks was the voice-over IP (VoIP) telephone. Because so many other Ethernet devices are able to use this convenient source of power (RFID readers, chargers for PDAs, mobile phones, or even laptops), the IEEE 802.3af standard includes an optional feature called power classification. This allows the PSE to manage its power budget more closely. **Table 3** lists the different power classes for which a PD can be provisioned, and their corresponding classification signatures.

To implement the optional power classification method, the PSE applies a probing voltage of 14.5V to 20.5V. In response, the PD exhibits a signature (classification current), indicating back to the PSE the maximum power the PD can draw. That information enables the PSE switch to manage the maximum power it delivers to the connected PDs at any given time.

By selecting a proper PSE controller IC, you could implement another feature that is outside of the IEEE 802.3af standard: a hard limit on the PSE's output power per port. Unless the deployment administrator can guarantee that no PD will ever be swapped out for one that dissipates more power, the switch's expected power budget can occasionally be exceeded. In that case, the PSE will refuse to power the port unless the PD power classification is met.

Another feature handy in emergencies would be an ability for the PSA to prioritize which ports receive power first, or which ports should be disconnected first when the UPS or backup generator begins to run out of energy. The switch could then maintain power for the most important Ethernet ports. Such ports might include E911 telephones, badge readers for access, certain surveillance cameras or access points, or other revenue-generating data circuits.

Table 2. Detection of any criterion below by the midspan or endpoint PSE indicates that Ethernet device is an invalid PD.

Parameter	Conditions (V)	Range of Values
V-I slope	2.7 to 10.1	Either >45kΩ or <12kΩ
Input capacitance	2.7 to 10.1	>10µF

Table 3. Five classes for PD power classification and their classification signatures.

Class	Conditions (V)	Classification Current (mA)	PD Power Range (W)
0 (Default)	14.5 to 20.5	0 to 4	0.44 to 12.95
1	14.5 to 20.5	9 to 12	0.44 to 3.84
2	14.5 to 20.5	17 to 20	3.84 to 6.49
3	14.5 to 20.5	26 to 30	6.49 to 12.95
4 (Reserved for future use)	—	—	—

The presence of such fail-safe features within the PSE controller IC, either hardwired or software-configurable, can help manage the power budget during emergencies. Consequently, look for a software-configurable PSE controller IC.

Detecting disconnected PDs

After a PSE applies power to a PD, it must monitor the PD for a "maintain power" signature in accordance with the IEEE 802.3af standard. The PSE must also detect whether the PD has been disconnected. The standard defines both AC and DC methods for detecting a PD disconnect. Consider, for example, that a PD has been disconnected and a legacy Ethernet device immediately plugged into the same RJ-45 jack on the switch. If 48VDC power is not quickly disconnected after the PD is removed, the legacy device may be damaged.

AC-impedance measurements performed on a PD are generally more accurate than pure DC-resistance measurements. A small, common-mode AC voltage is sent down the Ethernet link simultaneously with the data signals and 48VDC. You then measure the AC current and calculate the resulting port impedance, which (if the PD has not been disconnected) should be less than 26.25kΩ. The frequency for this AC voltage must be between 1MHz and 100MHz. For the many other details pertaining to DC and AC methods of disconnect detection, the designer should consult the IEEE 802.3af standard. Regardless of the method chosen, the measurement must be made quickly and the power removed quickly thereafter.

Advanced features in silicon

Among the multiport PSE silicon chips now available, the most common are PSE controllers that control inline power to four ports. Look for I^2C^{TM}-compatible, serial-interface capability with programmable registers that provide the option of use with an MCU. Some of the advanced features residing in various operating modes are now important for emergency reasons, an importance that was magnified after 9/11/01.

Operational modes offered by the MAX5935, for instance, include automatic, semiautomatic, manual, shutdown, and debug mode. Automatic mode allows the device to operate without software supervision. Semiautomatic mode (on request) continuously detects and classifies a device connected to a port, but does not apply power to that port until directed by software. Manual mode, useful in system diagnostics, allows complete control of the device by software. Shutdown mode terminates all activity and turns off power to the ports. Finally, debug mode allows detailed system diagnostics by fine-stepping through the device state machine.

Figure 3 is a simplified example of a PoE system design, illustrating PSE and PD connections using Gigabit Ethernet. Because Gigabit Ethernet does not work with midspan power injection, the 100/10M Ethernet modes can only connect to an endpoint PSE switch. (The MAX5940 PD-interface controller does not need a diode bridge, yet it operates with one if required.) Today's PD-interface controller ICs (such as the MAX5941 and MAX5942) include a pulse-width modulation (PWM) controller, even though the PD usually includes a DC/DC converter.

Effective IM2 products estimation for two-tone and W-CDMA modulated blockers in 3GPP direct-conversion receivers

*As third-generation (3G) wireless networks are currently expanding in Japan (IMT-2000), Europe (UMTS), and the US (cdma2000), the need for low-cost, low-power consumption, and low form-factor user equipment (UE) is becoming important for the commercial development of 3G mobile handsets. The direct-conversion receiver architecture, with the proper use of silicon processes, circuit design techniques, and architecture implementation, represents a promising system solution for highly integrated platforms for 3G handsets. In this article, we present a commercially available, fully integrated, zero-IF receiver solution for 3G radios (**Figure 1**). The receiver-input, second-order intercept point (IIP2) requirement is discussed extensively in this paper, as it is a key specification for a direct-conversion receiver. Measurements, simulations, and calculations are presented specifically on this topic.*

The direct-conversion receiver architecture

As seen in Figure 1, direct-conversion or zero-IF receiver architecture enables the pathway for a full on-chip integration of the receiver. This is because the signal is directly demodulated to baseband I and Q signals. In a 3G, W-CDMA FDD (full-duplex) operation mode, only an external duplexer is needed for separation between Rx and Tx sections. Furthermore, the post-LNA RF filter is required in a FDD radio to reject out-of-band blockers and transmitter leakage at demodulator input. This happens due to finite duplexer Tx-Rx isolation. In a zero-IF receiver IC, channel selectivity is achieved at baseband by on-chip, low-pass filters. Following the channel filtering, I/Q signals at baseband are amplified by variable-gain amplifiers (VGAs) before they get digitized in the analog baseband section of the radio modem IC. Design considerations for direct-conversion receivers have been studied thoroughly [1, 2].

In *Second-order distortion effects*, we present and discuss all critical sources leading to the generation of second-order nonlinearity products in the zero-IF, receiver-IC downconverter. In *IIP2 derivation*, we provide a detailed review of the second-order, input-intercept point (IIP2) derivation. Then, in the last two sections, we tackle specifically the estimation of true IM2 products and the

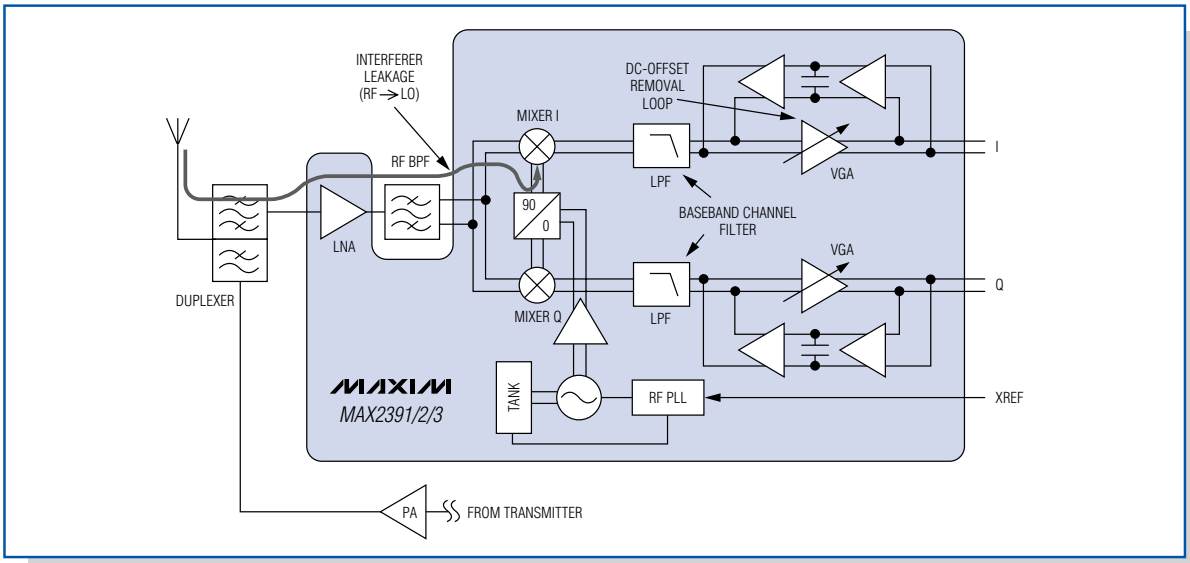

Figure 1. This direct-conversion receiver IC is a fully integrated, zero-IF receiver solution for 3GPP, FDD handset radios.

minimum IIP2 requirements for a 3GPP zero-IF receiver, based on the specified 3G standard test cases [3].

Second-order distortion effects

In a zero-IF receiver, second-order intermodulation products (IM2) have been shown to present a problematic source of interference [1]. Care must be taken to minimize the level of these products in the receiver's baseband channel. In a zero-IF receiver, the front-end, second-order nonlinearity demodulates the AM components of an amplitude-modulated blocker down to baseband. These second-order IM2 products consist of the squared version of the blocker envelope. Therefore, the bandwidth of these undesirable spectral components at baseband can be up to twice the bandwidth of the blocker's amplitude envelope. Depending on the desired signal modulation bandwidth at baseband, these IM2 products contribute partially, or fully to the degradation of the overall receiver's jamming margin.

The IM2 distortion products we are discussing here are those which occur in the downconverter section of a zero-IF receiver. This is because the low-frequency IM2 products in the LNA are normally filtered out by AC-coupling or bandpass filtering between the LNA and the mixer blocks. There are many different mechanisms responsible for the generation of IM2 products in a zero-IF receiver [4]. However, it is important to present here the two main IM2 generation mechanisms.

RF self-mixing

RF self-mixing occurs because of the imperfect, hard-switching I-V characteristic of the commutating stage in a zero-IF receiver mixer, and because the RF signal is leaking into the LO port due to parasitic coupling. The imperfect hard switching happens in a mixer when it is driven with low LO powers and, therefore, it behaves more like a linear multiplier. As a result, in the presence of an RF-to-LO leakage component at the LO port (Figure 1), the zero-IF mixer's output contains a signal that is proportional to both the square of the input signal and the RF-to-LO coupling factor. Consequently, second-order IM products are generated at baseband. When RF signal leaking to the LO port is a strong blocker, this is quite detrimental to receiver performance.

Downconverter RF-stage, second-order nonlinearity and LO-stage, switching-pairs mismatches

Upon the introduction of a strong CW or modulated blocker at the I/Q mixer inputs in a zero-IF receiver, the second-order nonlinearity in the active devices of the mixer transconductor or RF stage generates low-frequency IM2 products. These products, along with the desired RF signal and the blocker, are part of the transconductor-stage output currents. In a perfectly balanced mixer, including perfectly matched mixer loads or devices in the switching pairs or LO stage, the equivalent differential IM2 products are translated to high frequencies. Also, the equivalent common-mode IM2 products are canceled out at the mixer differential output. However, in addition to the deviation of the LO duty cycle from 50%, the mismatches that exist in the LO-stage devices result in a direct low-frequency leakage gain that is presented to the low-frequency IM2 products. As a result, these products get translated to I/Q mixers' baseband outputs.

It is important to note that previously we assumed that the downconverter section in a zero-IF receiver is the main limiting block in IM2 product suppression. This is true if the baseband stages following the I/Q mixers have high common-mode suppression (>60dB).

IIP2 derivation

The weakly nonlinear characteristics of a receiver front-end can be presented as:

$$V_O(t) = a_1 \times V_i(t) + a_2 \times V_i(t)^3 + L \qquad \text{(Eq 1)}$$

To express the second-order input intercept point (IIP2) based on two-tone derivation, the input signal to the receiver in **Figure 2** is expressed as $V_i(t) = A \times \cos(\omega_1 t) + A \times \cos(\omega_2 t)$, with a total two-tone power equal to A^2/R. The second-order distortion products at the receiver front-end are derived as:

$$a_2 \times V_i(t)^2 = a_2 \times A^2 \times \qquad \text{(Eq 2)}$$
$$[1 + \cos((\omega_1 - \omega_2)t) + \cos((\omega_1 + \omega_2)t) +$$
$$(\cos(2\omega_1 t)/2) + (\cos(2\omega_2 t)/2)]$$

The resultant output IM2 products at $(f_1 + f_2)$ and $(f_1 - f_2)$, including the resulting DC offset, are expressed as:

$$a_2 \times A^2 \times [1 + \cos((\omega_1 - \omega_2)t) + \qquad \text{(Eq 3)}$$
$$\cos((\omega_1 + \omega_2)t)]$$

The total power in the equation 3 output IM2 products, referred to as system impedance (R), is calculated as:

$$|a_2|^2 \times A^4 \times \left(\frac{1}{R} + \frac{1}{2R} + \frac{1}{2R}\right) = \qquad \text{(Eq 4)}$$
$$2 \times |a_2|^2 \times \frac{A^4}{R}$$

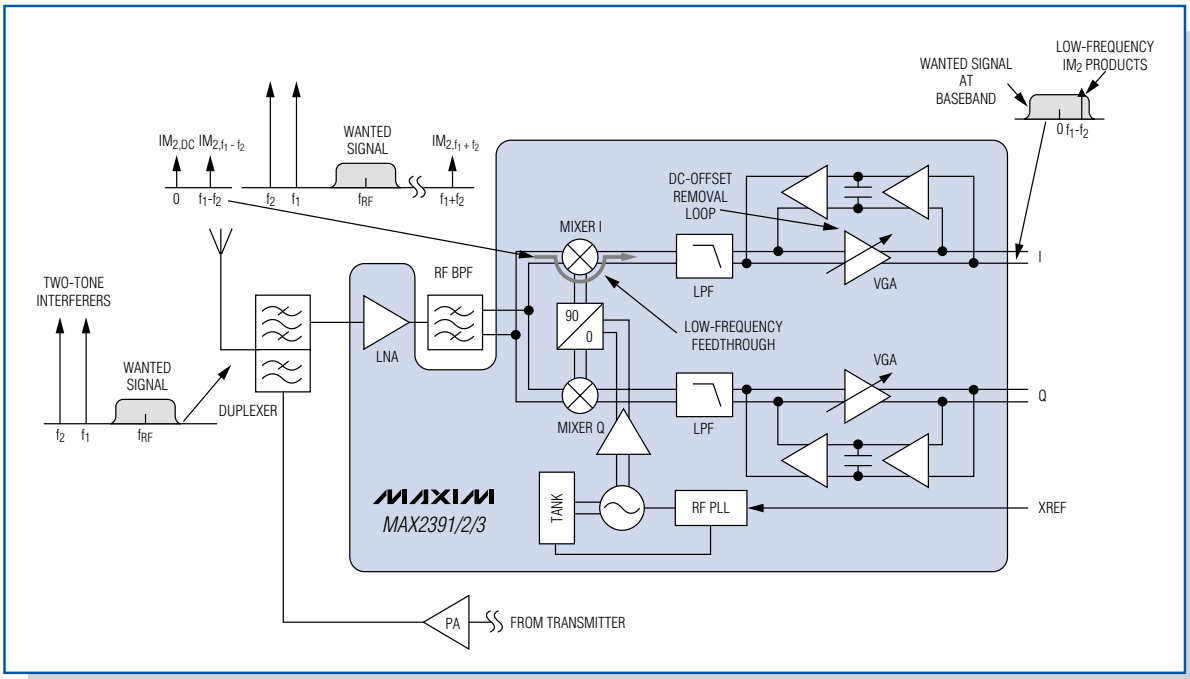

Figure 2. Second-order intermodulation distortion occurs due to the two-tone blocker in the zero-IF receiver.

At the IIP2 power level, the total input signal power is defined as equal to the total power in the output IM2 products (equation 4) after being referred to the input. This is done through dividing by the gain factor, $|a_1|^2$. As a result, we can write that:

$$A_{IIP2}^2/R = 2 \times \left|\frac{a_2}{a_1}\right|^2 \times \frac{A_{IIP2}^4}{R} \Rightarrow \qquad \text{(Eq 5)}$$

$$IIP2 = IIP2^2 \Big/ \left[\left|\frac{a_1}{a_2}\right|^2 \times \frac{1}{2R}\right] \Rightarrow$$

$$IIP2 = \left|\frac{a_1}{a_2}\right|^2 \times \frac{1}{2R}$$

Based on a total two-tone input power equal to $P_{2T} = A^2/R$, the total power level of the IM2 products (equation 4) referred to the receiver input can be expressed as:

$$P_{IM2} = 2 \times \left|\frac{a_2}{a_1}\right|^2 \times \frac{A^4}{R} = \frac{P_{2T}^2}{IIP2} \Rightarrow \qquad \text{(Eq 6)}$$

$$P_{IM2}(dBm) = 2 \times P_{2T}(dBm) - IIP2(dBm)$$

It is important to note that in equation 4 the resulting IM2 products' total power level is composed of 50% (-3dB) IM2 product at DC, 25% (-6dB) IM2 product at $(f_1 - f_2)$, and 25% (-6dB) IM2 product at $(f_1 + f_2)$. Therefore, the power level of the IM2 product at $(f_1 - f_2)$ can be derived from equations 4 and 6 as:

$$P_{IM2,(f1-f2)}(dbm) = 2 \times P_{2T} - IIP2 - 6dB \Rightarrow$$

$$P_{IM2,(f1-f2)}(dBm) = 2 \times P_{1T}(dBm) - IIP2(dBm) \quad \text{(Eq 7)}$$

where power level per tone (P_{1T} at f_1 or f_2) is 50% of the total two-tone power, $P_{1T}(dBm) = P_{2T}(dBm) - 3dB$.

Effective, low-frequency IM2 products

In a 3GPP W-CDMA radio, the worst-case interferers at receiver input are not two-tone type, but wideband digitally modulated-type blockers. Therefore, to derive the required receiver IIP2 for a certain desired BER performance, it is important to estimate the effective low-frequency IM2 products based on a modulated blocker. It is also necessary to understand the nature of the modulated blocker, specifically its nonconstant envelope. This is because the envelope gets stripped off the RF blocker in the front-end, second-order nonlinearity and gets translated to baseband with a squared version of the envelope. The two major modulated blockers in a 3GPP W-CDMA receiver are presented in 3G standard test cases, 7.3.1 and 7.6.1 [3]. The first test case, 7.3.1, specifies the minimum required sensitivity for BER<10^{-3}, while the transmitted uplink signal (UL) is at maximum power level (+24dBm) at the antenna. The second test

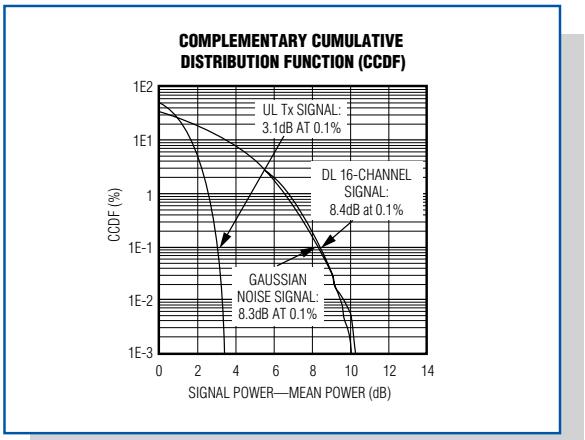

Figure 3. CCDFs of a UL reference channel and a DL 16-channel blocker are compared to Gaussian noise signal CCDF.

case, 7.6.1, specifies the minimum-required receive-signal level at the antenna connector for BER<10^{-3} in the presence of a modulated downlink (DL) -44dBm blocker. This is at 15MHz offset from the desired signal, while the transmitted UL power at the antenna is +20dBm.

The UL-reference measurement channel (12.2kbps) structure, which represents the transmitted uplink signal at the antenna of a 3G W-CDMA handset, is described in table A.1 of the 3GPP standard document [3]. It consists of a dedicated physical-data channel (DPDCH) and a dedicated physical-control channel (DPCCH). In the radio modem section, both DPDCH and DPCCH channels are spread to 3.84Mcps, scaled to the appropriate power ratio (DPCCH/DPDCH = -5.46dB), HPSK scrambled, and filtered by a 1.92MHz root-raised-cosine (RRC) filter with roll-off factor α = 0.22 [5]. Conversely, the forward-channel modulated blocker at 15MHz offset from the desired channel consists of the common channels needed for tests (Table C.7 in [3]) and 16 dedicated data channels (Table C.6 in [3]). The signal is QPSK encoded, spread to 3.84Mcps, complex scrambled, and filtered by a RRC filter similar to that used for UL signal [5]. Both signals have a -3dB bandwidth equal to 3.84MHz at RF, and 99% of total signal power is within a bandwidth of 4.12MHz (-6dB BW). To understand the nature of the envelope of either the modulated UL-transmitted (Tx) signal or the modulated DL 16-channel signal, and to estimate the effective IM2 products *due to each one of them* in a W-CDMA receiver, it is important to study first the power statistics of each signal. It is also essential to estimate the effective IM2 products as they each exist in a W-CDMA zero-IF receiver. This is represented by the complementary cumulative-distribution function (CCDF) that provides the signal's peak-average power ratio (PAR) vs. probability. **Figure 3** shows ADS™-simulated CCDFs of the UL-transmitted signal and the DL 16-channel signal as compared to the CCDF of a Gaussian noise signal.

It is worth noting from Figure 3 that the PAR at 0.1% probability of the UL-reference channel, based on one transmitted DPDCH, is equal to 3.1dB. On the other hand, the DL blocker at the 15MHz offset, which contains 16 dedicated traffic channels, has an 8.4dB PAR at 0.1% that is almost equal to that of a Gaussian noise signal. It will be shown later that the effective, low-frequency IM2 product estimation differs between the two standard test

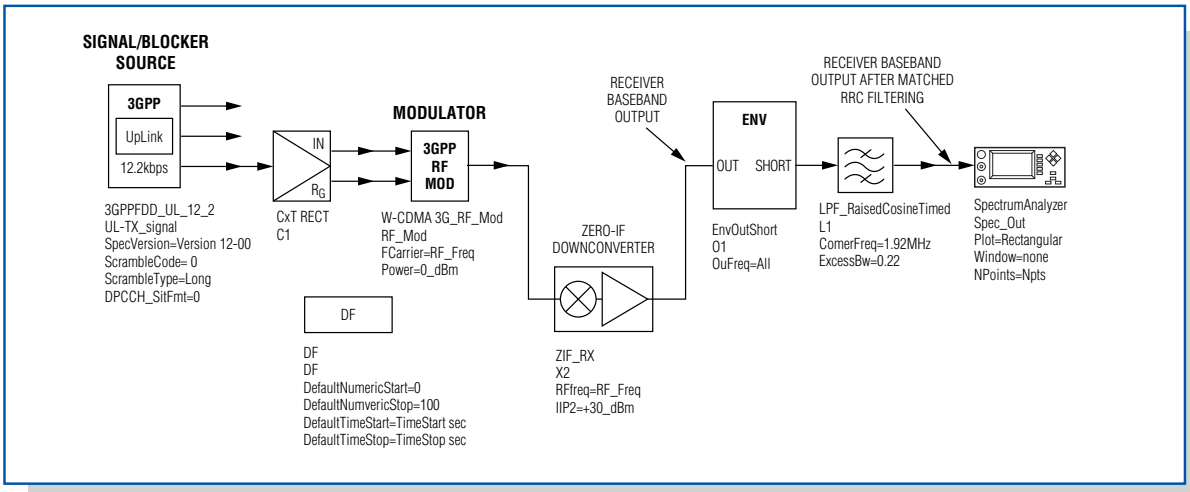

Figure 4. An ADS template details IM2 products estimation.

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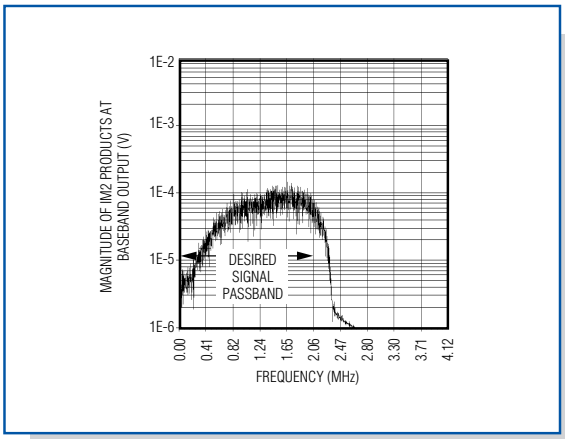

Figure 5. Simulated RRC-filtered IM2 products at zero-IF receiver output are produced due to an UL Tx blocker.

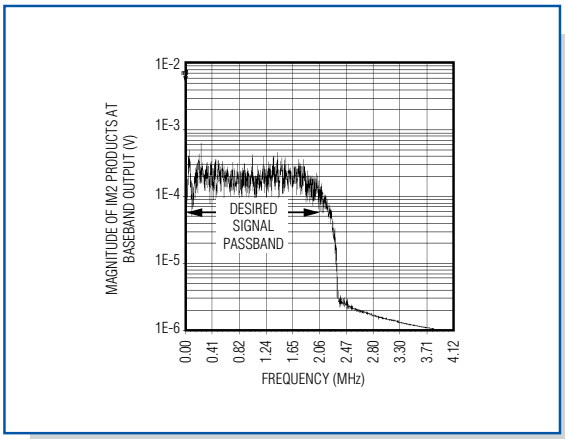

Figure 6. Simulated RRC-filtered IM2 products at zero-IF receiver output occur due to a DL 16-channel blocker.

cases. This is because of the PAR discrepancy between the two different blockers.

An ADS IM2 simulation template was created to investigate the IM2 products due to a modulated blocker at the input of a W-CDMA zero-IF receiver (**Figure 4**). The IM2 products were filtered by an RRC filter, which is matched to the base station transmitter RRC filter. The resulting low-frequency IM2 products were measured in simulation with the 0Hz to 2.06MHz desired signal bandwidth at baseband, which is half the signal's 99% power BW at RF.

In **Figures 5** and **6**, simulated IM2 product magnitude spectrums at the baseband output of a zero-IF downconverter (after matched RRC filtering) is presented for both the W-CDMA UL reference measurement channel (12.2kbps) and for the W-CDMA DL 16-channel blocker, respectively. In the ADS template and for simulation purposes only, we used a modulated blocker power equal to 0dBm and a zero-IF downconverter IIP2 equal to +30dBm. The resulting low-frequency IM2-product power level for a 0dBm, W-CDMA UL Tx signal, integrated over the desired signal passband of 1kHz to 2.06MHz, is equal to -43.7dBm. In addition, the DC offset due to second-order nonlinearity is equal to 5mV, which is equivalent to -33dBm into 50W (Figure 5). On the other hand, the resulting IM2 products' power level for a 0dBm, W-CDMA DL 16-channel blocker, integrated over the desired signal passband of 1kHz to 2.06MHz, is equal to -33.1dBm. The resulting DC offset due to second-order nonlinearity is also equal to 5mV (Figure 6).

Returning to equation 6 and assuming a total power level for a two-tone blocker of 0dBm at zero-IF downconverter input, the total IM2-product power level referred to receiver input is calculated as $P_{IM2}(dBm) = 2 \times P_{2T}(dBm) - IIP_2(dBm) = -30dBm$. The resulting DC-offset level is -33dBm and the power level of the IM2 product at $(f_1 - f_2)$ is -36dBm, based on equations 4 and 7, respectively. Therefore, it can concluded that the integrated, low-frequency, IM2-product power level over the 1kHz to 2.06MHz band, due to a 0dBm, UL Tx blocker, is 7.7dB lower than the low-frequency, $(f_1 - f_2)$, IM2-product power level due to a two-tone 0dBm blocker. Similarly, the equivalent total low-frequency IM2 products' power level due to a 0dBm DL 16-channel blocker is 2.9dB higher than the low-frequency, $(f_1 - f_2)$, IM2-product power level due to a 0dBm two-tone blocker. The total effective IM2-product power levels based on the previous results are summarized in the following equations:

For the UL reference channel or Tx-blocker case,

$$P_{IM2,UL\_TX}(dBm) = \quad \text{(Eq 8)}$$
$$2 \times P_{UL\_TX}(dBm) - IIP2(dBm) - 13.7dB =$$
$$2 \times P_{1T}(dBm) - IIP2(dBm) - 7.7dB$$

For the DL 16-channel blocker case,

$$P_{IM2,DL\_16Ch}(dBm) = \quad \text{(Eq 9)}$$
$$2 \times P_{DL\_16Ch}(dBm) - IIP2(dBm) - 3.1dB =$$
$$2 \times P_{1T}(dBm) - IIP2(dBm) + 2.9dB$$

In equations 8 and 9, the power level per tone (P_{1T} at f_1 or f_2) is 50% of the total power level (P_{2T}) of a two-tone blocker having the same power level as the modulated blocker, $P_{1T}(dBm) = P_{2T}(dBm) - 3dB = P_{UL\_TX/DS\_16Ch}(dBm) - 3dB$. It is important to note that the -13.7dB reduction

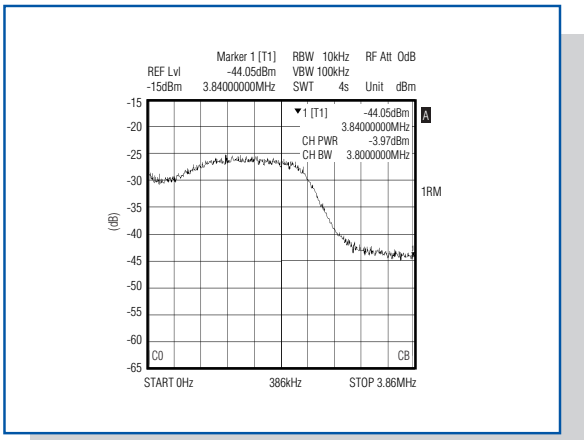

Figure 7. Measured IM2 products, without RRC filtering, at zero-IF receiver output transpire due to an UL Tx blocker.

factor relative to the total IM2-product level estimate in equation 8 is very similar to the factor obtained in the results presented in reference [6]. Furthermore, the results presented by equation 8 have been verified through lab measurements done on a zero-IF receiver device with the part shown in Figure 1. The measured IM2 products at baseband due to UL Tx blocker (Figure 7) show similar spectrum characteristics to the simulated IM2 products shown in Figure 5. The measured spectrum components close to DC in **Figure 7** are larger than the corresponding simulated components in Figure 5. This is due to the additional downconverted phase noise close to DC in the actual measured zero-IF receiver.

Minimum IIP2 requirements for a W-CDMA receiver

In the following section, the required minimum IIP2 for a W-CDMA, zero-IF receiver for both test cases, 7.3.1 and 7.6.1, is derived based on equations 8 and 9, respectively. All IIP2 calculations are done in reference to the receiver LNA input.

3GPP standard test case 7.3.1

• In FDD mode, the estimated maximum UL Tx signal leakage at the LNA input is -24dBm ($P_{UL\_TX,\ LNA}$ = PA power at duplexer - $Duplexer\_Isolation_{TX\_RX}$, min = +26dBm - 50dB = -24dBm). The worst-case insertion loss (IL) of the duplexer before the LNA is assumed equal to -2dB. In a 3GPP, IMT-band radio handset, the Tx-leakage frequency offset relative to the desired Rx signal frequency is 190MHz.

• It was shown in [7] that, for a required traffic-channel sensitivity of -117dBm/3.84MHz, the required minimum E_b/N_t is 7dB after decoding and despreading of the desired traffic channel. In test case 7.3.1, which specifies the minimum required traffic-channel sensitivity for BER<10^{-3}, N_t is assumed to be purely noise (N_O) due to receiver NF. For a chip rate of 3.84Mcps and a user bit rate of 12.2kbps, the processing gain is Gp = 10log(3.84Mcps/12.2kbps) = 25dB. We can calculate that the maximum allowable noise power (P_N) due to receiver NF is $P_N = P_{Sensitivity} + Gp - E_b/N_t$ = -117dBm + 25dB - 7dB = -99dBm.

• At minimum sensitivity level, it is required that the low-frequency IM2 products due to UL Tx-leakage blocker do not desensitize the receiver. The resulting DC offset due to IIP2 has no effect because, in a W-CDMA zero-IF receiver, DC offsets are typically rejected on-chip. If it is assumed that the total power level of low-frequency IM2 products needs to be at least 11dB lower than P_N (maximum of 0.3dB receiver desensitization), the maximum allowable input IM2 due to UL Tx-leakage blocker, referred to receiver LNA input, can be estimated using: $P_{IM2,UL\_TX} = P_N$ - 11dB - $I_{Lduplexer} \le$ -99dBm - 11dB - 2dB = -112dBm.

• The receiver IIP2,TX at Tx offset (190MHz), referred to receiver LNA input, is calculated using equation 8: P_{IM2,UL_TX}(dBm) = 2 × $P_{UL\_TX\_LNA}$(dBm) - $IIP_{2,TX}$(dBm) - 13.7dB ⇒ $IIP_{2,TX}$(dBM) ≥ +50dBm.

3GPP standard test case 7.6.1

• In this test case, the desired signal is 3dB above the minimum sensitivity specified in test case 7.3.1. Hence, the maximum allowable noise plus interference power level is -96dBm. This is 3dB higher than level calculated in the previous test case. Assuming the same level of receiver noise (-99dBm), the maximum-allowable interference power level is -96dBm - 3dB = -99dBm.

• The total interference power due to the W-CDMA DL, 16-channel blocker, 15MHz offset from the desired signal is assumed to be divided mainly between three products. These are phase-noise reciprocal mixing (25% or -6dB), blocker level at receiver output after on-chip filtering (25% or -6dB), and low-frequency IM2 products due to this blocker (50% or -3dB). Hence, we can estimate the maximum allowable input IM2 products' level due to DL blocker, referred to receiver LNA input, using: P_{IM2,DL_16Ch} = P_N - 3dB - $I_{Lduplexer} \le$ -99dBm - 3dB - 2dB = -104dBm. The low-frequency IM2 products due to the UL Tx-leakage signal have been neglected, because the UL Tx power in this test has been reduced by 4dB relative to the level specified in test case 7.3.1.

• In this test case, the specified modulated blocker level is equal to -44dBm at antenna; hence, with -2dB IL in duplexer, the level of the blocker at LNA input, $P_{DL\_16Ch,\ LNA}$, is -46dBm.

• The receiver IIP2 (15MHz) at 15MHz offset, referred to receiver LNA input, is calculated using equation 9: $P_{IM2,DS\_16Ch}(dBm) = 2 \times P_{DL\_16Ch,LNA}(dBm) - IPP_{2,(15MHz)}(dBm) - 3.1dB \Rightarrow IIP_{2,(15Mhz)}(dBm) \geq +9dBm$.

When all are referred to LNA input, it is noteworthy that the required zero-IF receiver IIP2 (TX) at the UL Tx frequency offset is higher than the required IIP2 (15MHz) at the DL 16-channel blocker frequency offset. When translating the IIP2 (TX) requirement to the I/Q mixers inputs, this imposes the need for mixers' IIP2 (I/Q_mixer) to be larger than +60dBm. However, this requirement can be relaxed by the use of the post-LNA filter, which provides selectivity at the Tx-leakage offset frequency [8].

Conclusion

This article presented simulations, calculations, and measurements to estimate the required zero-IF receiver IIP2 in the presence of a modulated W-CDMA blocker. Depending on the envelope nature of the modulated blocker, it has been shown that the resulting low-frequency IM2 products' level at baseband can be lower or higher than the low-frequency IM2 beat-tone level that results from an equivalent two-tone blocker.

A similar article appeared in the April, 2004 issue of RF Design.

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